5G-XHaul

Dynamically Reconfigurable Optical-Wireless Back-haul/Fronthaul with Cognitive Control Plane for Small Cells and Cloud-RANs

D4.1 Optical backhauling supporting convergence of Fibre optic & mm-Wave communications

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Executive Summary

The 5G-XHaul solution leverages an optical transport solution to support 5G networking and address its high bandwidth connectivity requirements. The Time Shared Optical Network (TSON) metro network is a proven active Wavelength Division Multiplexing (WDM) solution which is providing variable sub-wavelength switching granularity and the ability to dynamically allocate optical bandwidth elastically. This deliverable studies the TSON 5G-XHaul implementation, to address the varying fronthauling capabilities needed by the different Remote Radio Head (RRH) systems and the backhaul (BH) requirements and interfaces of the 5G-XHaul network.

1   Introduction

The 5G-XHaul solution proposes converged optical and wireless networks technologies to shape a flexible transport infrastructure. It proposes a new Centralised Radio Access Network (C-RAN) architecture supporting both Backhaul (BH) and Fronthaul (FH) functionalities. In addition, 5G networks require high bandwidth and sub-millisecond end-to-end latency. We have proposed the state of the art Time-Shared Optical Network (TSON) technology as an active optical solution to offer high bandwidth and low-latency connectivity in support of the requirements of 5G technology and provision jointly optical BH and FH services. The TSON baseline technology has been extended over the course of the 5G-XHaul project to provide synchronisation capabilities as well as to support multi-Ethernet clients for BH, and Common Public Radio Interface (CPRI) integration for FH services.

In this deliverable, we first study the TSON technology in Section 2. In the three following sections we introduce the TSON extensions for 5G-XHaul. Section 3 discusses how we managed to tackle the synchronisation issue. Section 4 demonstrates the TSON extensions needed to support multi-Ethernet clients for BH services. Section 5 reveals the TSON CPRI extension for FH. In Section 6, we study the TSON demonstration configuration based on input provided by the planned demonstrations in WP5. Although during the lifetime of this WP we faced several technical challenges we have managed to solve all technical issues successfully. Section 7 talks about these technical issues. Finally, Section 8 summarises and concludes this document.

2   Time Shared Optical Network Technology

The 5G-XHaul solution uses the TSON technology [1] to support the varying degrees of bandwidth and latency requirements introduced by Radio Access Network (RAN) deployments. To this end, in 5G-XHaul we have proposed the use of a wavelength division multiplexed (WDM) optical metro network technology referred to as Times Shared Optical Network TSON. In this section, we discuss the TSON architecture, describe its capabilities, and present its evaluation results.

2.1   Generic TSON functionality/architecture

TSON is a multi-wavelength fully bi-directional synchronous and novel frame based flexible system. It delivers a flexible and statistically multiplexed optical network infrastructure and on-demand guaranteed time-shared multi-granular services. Its network implementation consists of field-programmable gate array (FPGA) optoelectronics platforms integrated with advanced optical components to enable high performance processing and transparent switching and transport [1] [2] [3]. TSON is a contention-less solution through the deployment of a central resource allocation engine of route, wavelength, and time assignment, responsible to set-up the sub-wavelength paths. A high-level view of the overall TSON architecture and how it can support the overall 5G-XHaul vison and architecture is shown in the figure below [4].
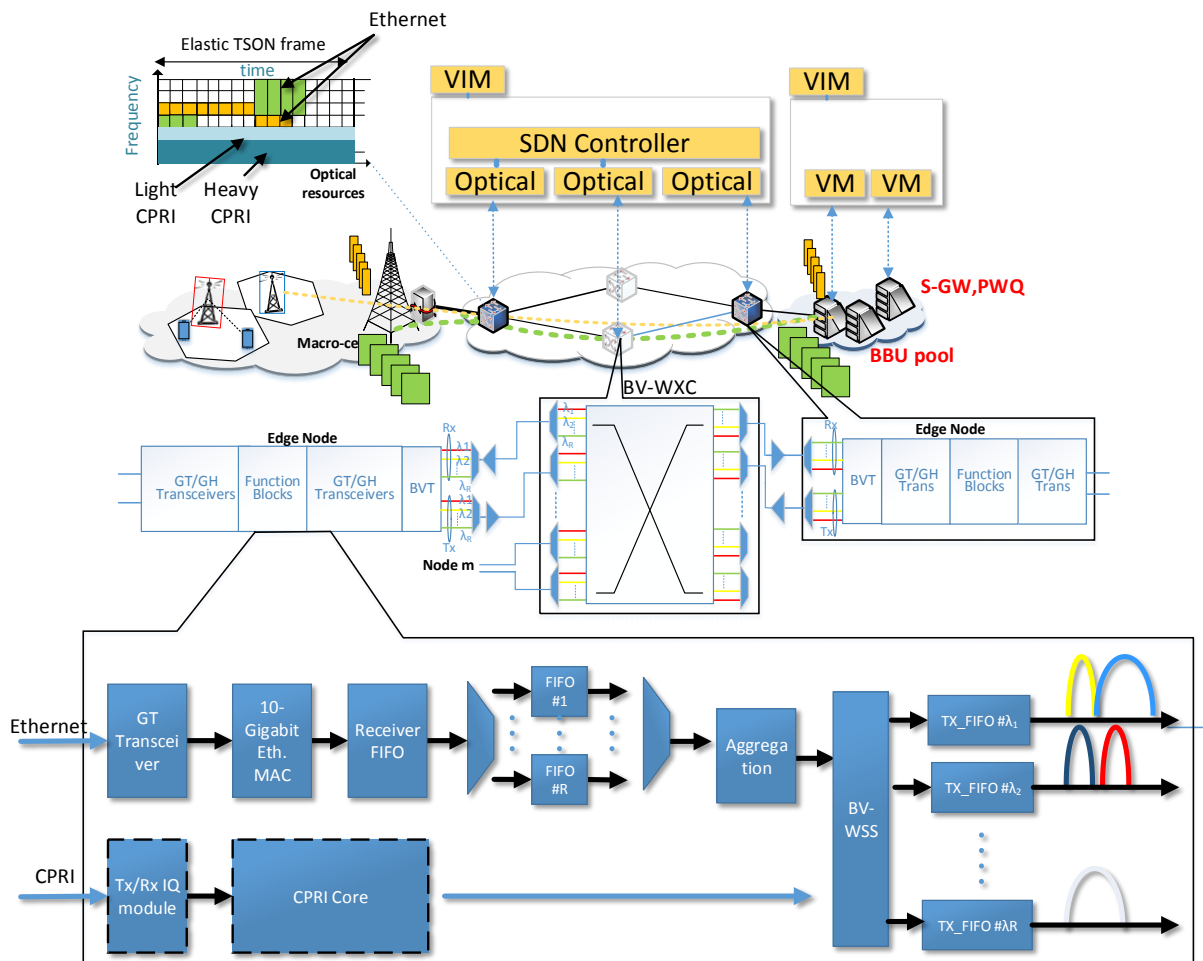
Figure 2-1: TSON architecture.

The TSON solution includes two different types of nodes, the edge and the core nodes, incorporating different functionality and level of complexity. TSON edge nodes provide the interfaces between wireless, Passive Optical Network (PON) and Data Centre (DC) domains to the optical domain and vice versa. Figure 2-2 shows the TSON edge architecture. The ingress TSON edge nodes are responsible for traffic aggregation

and mapping, while the egress edge nodes include the reverse functionality. To send and receive data, each TSON edge node uses four SFP+ transceivers, two 1310 nm 10 km reach for end-point server traffic and control, and two DWDM 80 km reach transceivers at 1544.72 nm and 1546.12 nm. The 1310 nm interfaces can be used to support both data and control traffic either separately or combined depending on whether out-of-band or in-band control is adopted. For more information on the TSON overall architecture and interfaces the interested reader is referred to deliverable D2.2 [4].
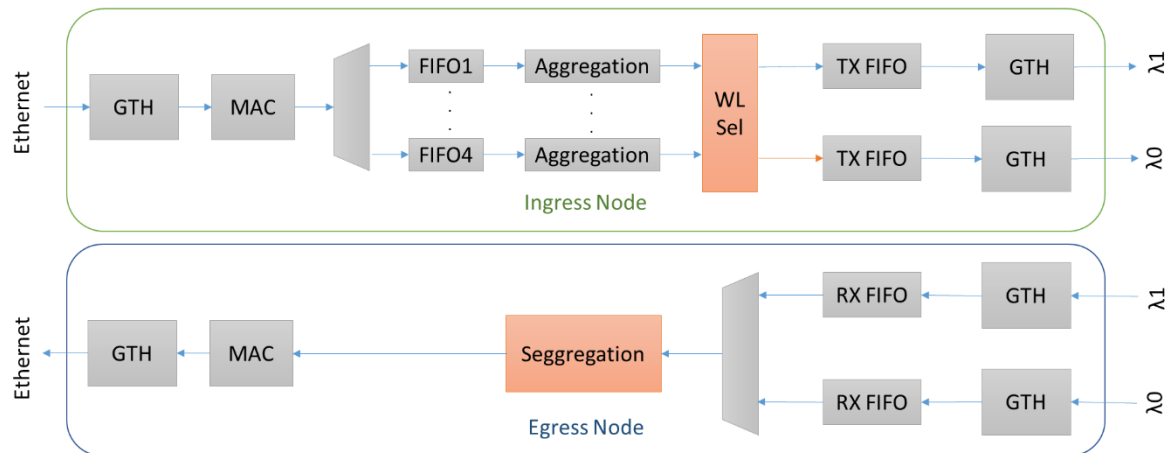

Figure 2-2: TSON edge node architecture.

When the ingress part of the edge node receives traffic, the FPGA waits to finish the processing of the current frame, and then starts to transmit time-slices based of optical bandwidth. The optical bandwidth allocated to the different services is not fixed but can be elastically defined based on the requirements of each service, as discussed in deliverable D2.2. Therefore, TSON can support elastic time and optical bandwidth allocation. As an example, in Figure 2-2, when the input traffic comprises Ethernet frames at the ingress part of the edge node, the Ethernet frames received at the 10 Gbps receiver are passed to the 10GE Medium Access Control (MAC); Then MAC discards the preambles and Frame Check Sequence (FCS), transmits the data to the Receiver (RX) in a first in first out (FIFO) manner and indicates whether the packet is good or not; the RX FIFO receives the data, waits for the good/bad indication from the MAC, and sends it to the DEMUX block if there is any valid data. The DEMUX analyses the Ethernet frame information (i.e. Destination MAC address, Source MAC address, etc.) and puts them in a different FIFO. After that, the FIFO does not send any data until the AGGREGATION gives a command; the register file of AGGREGATION, containing the Time-slice Allocation information, is updated by the Lookup Table (LUT) (this table stores information related to time-slice Allocation and the fast optical switch that is incorporated in the edge TSON node). The AGGREGATION module waits until the burst-length Ethernet frames are ready in the FIFO and the time-slice allocation is available, then it transmits the bursts with a suitable wavelength through the TX FIFO. For the egress part of the edge TSON node, when the 10 Gbps receiver receives a burst (time-slice), it drops the burst in the RX FIFO Lambda0/Lambda1; after the burst is completely received, the SEGREGATION block segregates the burst to Ethernet frames and transmits them to a TX FIFO. Every time the TX FIFO receives a complete Ethernet frame it sends it to the 10GE MAC. Finally, MAC passes the data to the 10 Gbps transmitter and transmits them out.

The TSON core nodes do not carry out any data processing but need to switch the traffic optically. Therefore, the FPGA-based TSON core node controls the fast optical switches to setup the path with a client's request. These nodes switch transparently the optical frames to the appropriate output port utilising the fast optical switching which in the core node as was also in the edge node case. The TSON core nodes adopt the wavelength selective architecture and as such require one switch per wavelength, to direct the incoming optical time-sliced signals towards the appropriate output ports, as defined by the control plane. The dimension of the space switch is defined by the number of fibres that are interconnected through the node. The TSON core node uses the same type of high performance FPGA boards for the ((Pb,La)(Zr,Ti)O3) (High-Speed PLZT Optical Switches) control. The FPGA LUTs are filled in by the control plane, through customised Ethernet communication carrying PLZT switching information, to be able to change the switch state per time-slice on the PLZT switches with the aim to establish and maintain optical paths across the TSON domain. The basic functions for the operation of TSON domains have been implemented in internal modules, within

the Software Defined Networking (SDN) controller, that cooperates for the on-demand provisioning of connectivity between TSON core and edge nodes. The interested reader can find a detailed description of the TSON control plane in the 5G-XHaul deliverable D3.1 [5].

TSON works in two different modes: Ethernet and Elastic bandwidth allocation mode. The Ethernet mode is for Ethernet based packets without any time-slicing. Elastic bandwidth allocation is based on time-slicing as described earlier in this section. Even though the latest TSON implementation is based on Xilinx Virtex7 board (156.25 MHz clock frequency), supporting multiple 10 Gbps (for control and transport) DWDM SFP+ transceivers, the architecture can support beyond 10 Gbps (i.e. 25, 40, 100 Gbps). For the optical layer, TSON relies on fast optical PLZT switches [3] having 10 ns switching speed as well as a set of active and passive components including Erbium Doped Fibre Amplifiers (EDFAs), MUX/DEMUXes, etc. TSON is designed and implemented as a novel frame-based, time multiplexing network solution, offering dynamic connectivity with fine granularity of bandwidth.

Although natively TSON allows handling of Ethernet frames, its configuration can support a broad range of framing structures and communication protocols including CPRI and Open Base Station Architecture Initiative (OBSAI), either natively or through their packetized versions.

2.2 TSON resource allocation capabilities

TSON is fully SDN enabled, and the parameters of TSON nodes are programmable by the controller, such as Quality of Transmission (QoT), overhead that is programmable from 0 to 39 KB, time-slice size that is programmable from 80 B to 31.25 KB, time-slice numbers in a frame that are programmable from 4 to 100, and time-slice allocation. Thus, when the client (e.g. operator, service provider) requests to setup a network service, after evaluating its requirements such as bit-rate, connectivity type, Quality of Service (QoS), and QoT by the network controller, the TSON nodes chose the corresponding QoT overhead size, Time-slice size, time-slice number and time-slice allocation to fulfil such requests to compose a dedicated network function slice of the node. In addition, TSON supports programmable traffic flow control, i.e. virtual LAN (VLAN), Dest MAC, Src MAC.

TSON offers a hierarchy of three levels of resource granularity: connections, frames, and time-slices, as illustrated in Figure 2-3. Connection refers to a sub-wavelength light path establishment between any two end points in the TSON domain. To improve statistical multiplexing of data units, each connection lasts for number of frames with minimum size of 1 ms. Each frame is divided into time-slices as the smallest units of network resource, i.e. the actual sub-lambda resources. The frame length and the number of time-slices inside a frame define the minimum granularity achievable by the TSON network [4]. The TSON framework offers a very flexible optical platform that supports sub-wavelength switching, frame lengths, varying from 64 ns to 25.6 µs and variable bit rates, spanning from of 30 Mbps up to several Gbps, with 30 Mbps step.
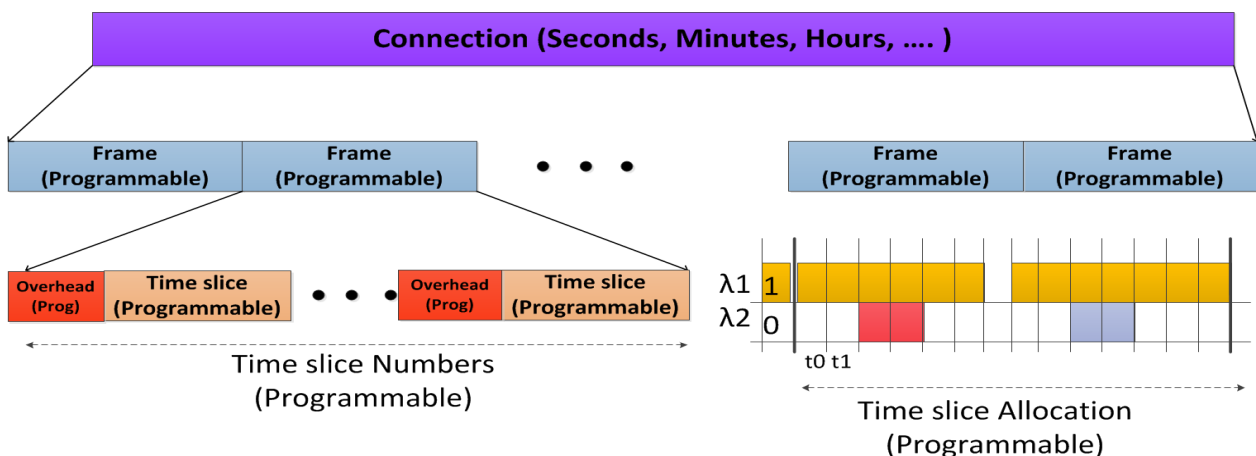

Figure 2-3 : Structure of connection, frame and burst [2].

2.3 TSON Evaluation

Figure 2-4 and Figure 2-5 show the TSON evaluation results obtained using Ethernet as an interface technology. This evaluation is based on latency and jitter analysis.

Figure 2-4 displays the impact of latency as a function of time-slots. As expected, the latency increases as the time-slice size increases because a higher number of packets are accumulated in a given time-slot. However, when the TSON node is in the Ethernet mode the minimum latency is 1.747 µs, while in Elastic bandwidth allocation mode, the latency ranges from 9.234 µs to 118.233 µs.

On the other end, Figure 2-5 shows the impact of jitter as a function of time-slices. The frame size is set to 1500B with 5 Gbps traffic. As the time-slice size grows, the percentage of traffic not received in a given time (e.g., 2 µs) decreases, but the percentage of traffic with more latency increases, thus increasing the jitter.

The minimum latency is 1.747 µs, while, in Elastic TDM mode, the latency ranges from 9.234 µs to 118.233 µs when the node is in Ethernet mode. In addition, as the time-slice duration increases, so does the jitter, and the number of packets not received at certain times increases.
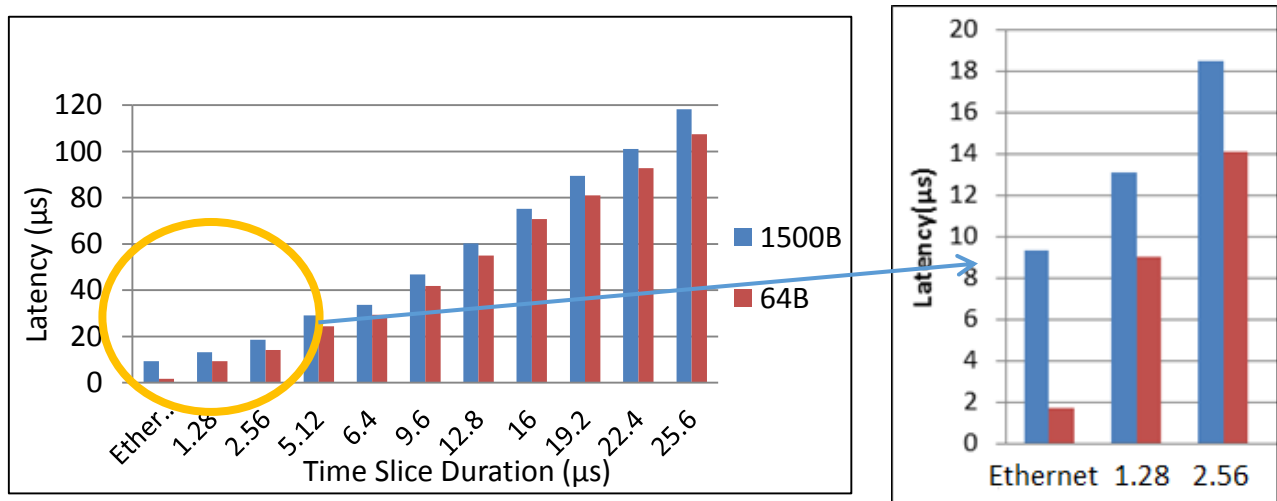

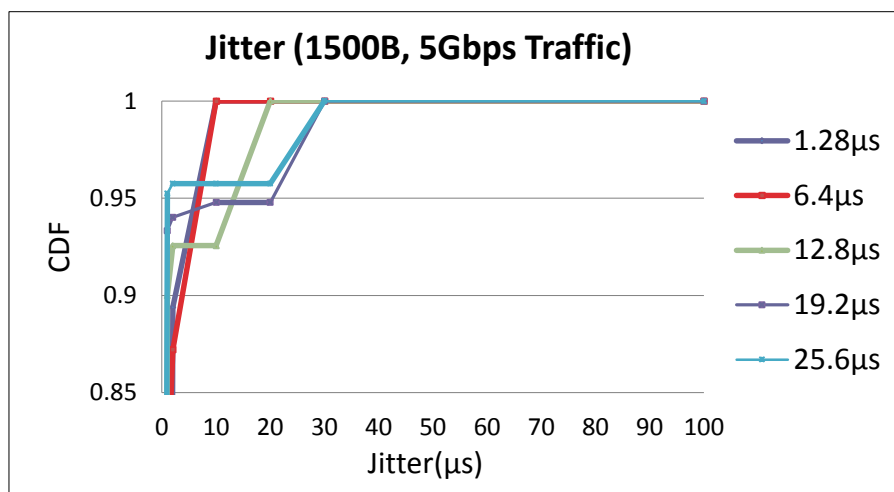**Figure 2-4: Latency vs. Time slice duration (1500B, 5 Gbps traffic).**

Figure 2-5: Jitter (1500B, 5 Gbps traffic).

3 TSON Synchronisation

To achieve high synchronisation accuracy over the network, accurate timestamps are required. Although TSON has its own synchronisation scheme [4], the TSON network requires global frame synchronisation among TSON nodes to meet the precision needed in the 5G-XHaul environment. The 5G-XHaul solution takes advantage of the IEEE-1588 v2 protocol [6] across heterogeneous domains. This solution needs to be at least a Transparent Clock (TC) for a given domain/node. This introduces the following requirements:

- The domain/node can measure the residence time of a 1588v2 packet inside the domain/node. This indicates: 1588 packets are recognised at the ingress, a timestamp is generated in the node, at the egress port the time is again measured, a residence time is computed "as egress-ingress time".

- The residence time is copied in a subsequent "Follow up" packet sent by the 1588 Master clock node.

- The synchronisation end-point will subtract the residence time from the follow up to this measurement of RTT in order to remove per domain jitter.

Applying the approach described above to a TSON domain means that the residence time is computed at the egress TSON node as the difference between its current time and the time when the packet enters the TSON ingress source node. Therefore, the TSON nodes need to be synchronised, being in principle a different synchronisation than that of 1588 v2. It is a synchronisation local to TSON that is required to compute the residence time in a meaningful way. In this scenario, the ingress time needs to be conveyed to the TSON egress node. Therefore, the time stamps need to be transmitted in-band to calculate the residence time.

There are two options for an FPGA design to be compliant with the IEEE-1588 v2 protocol:

3.1 External FPGA solution

Engaging a Network Interface Card (NIC) is the first and the most convenient option for the synchronisation as the external solution. As an example, Exablaze's ExaNIC GM is a combined IEEE-1588 v2 Protocol and ultra-low latency network card. The device is conveniently packaged in a PCIe card form factor with twin SFP+ ports, making it easy to install while saving valuable rack units [7]. In addition, the IEEE 802.1 Time Sensitive Networking (TSN) Task Group [8] is progressing a new generation of protocols for Ethernet to support time-sensitive networking with enhanced characteristics providing dramatically decreased and deterministic delays and delay variation, with better time synchronisation, and scalability to larger network configurations. The NIC card connects the FPGA to the network and handles synchronisation for the FPGA board. Figure 3-1 shows the combination of the NIC and FPGA which are both located on a server.
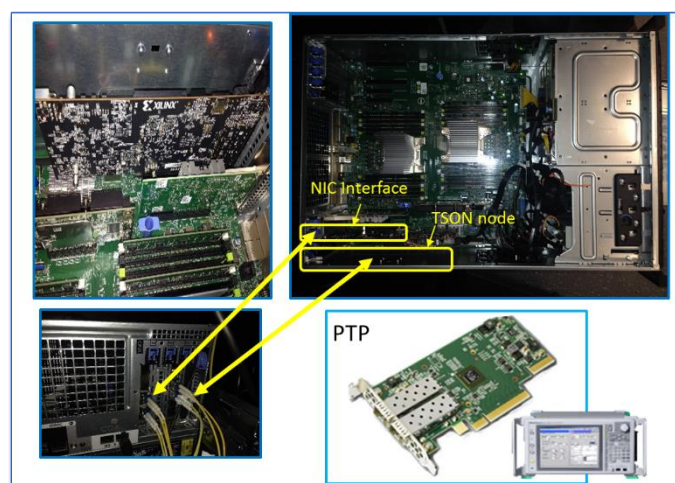

Figure 3-1: NIC and FPGA board on a server for synchronisation.

3.2 Internal FPGA solution

Xilinx 10 Gigabit Ethernet Subsystem IP core [9] supports high accuracy IEEE-1588-v2 1-step and 2-step timestamping on a 10GBASE-R network interface. Figure 3-2 shows the block diagram of the 10G Ethernet MAC subsystem. The subsystem IP core has three main sub IP cores: a MAC, a Physical layer (PCS/PMA), and a Timer for synchronisation. The time stamper unit for the transmit-side and the receiver-side are implemented inside the MAC and the PCS/PMA sub IP cores, respectively.

This subsystem synchronises the 1588 system timer in the selected format from the system timer clock domain into the subsystem clock domain for transmit and receive data paths. This guarantees high accuracy for the 1588 timestamps. The selected format is available in one of two Time-of-Day (ToD) and Correction Field timestamp formats. The subsystem supports both In-band and out-of-band timestamping methods. The system timer could be delivered to the FPGA board via available SMA user clock on the board.

As it can be seen in Figure 3-3, the Xilinx subsystem IP core does not support multiple IEEE-1588 v2 enabled subsystem instances [10]. In addition, as we mentioned before for the 5G-XHaul solution, the residence time needs to be computed at the egress TSON node as the difference between its current time and the time when the packet enters the TSON ingress source node. Therefore, the TSON nodes need to be synchronised and this in principle is different synchronisation than the synchronisation carried out by IEEE-1588 v2 even though the timing format – i.e. Time of Day (ToD) and Correction Field – is the same as in IEEE-1588 v2.
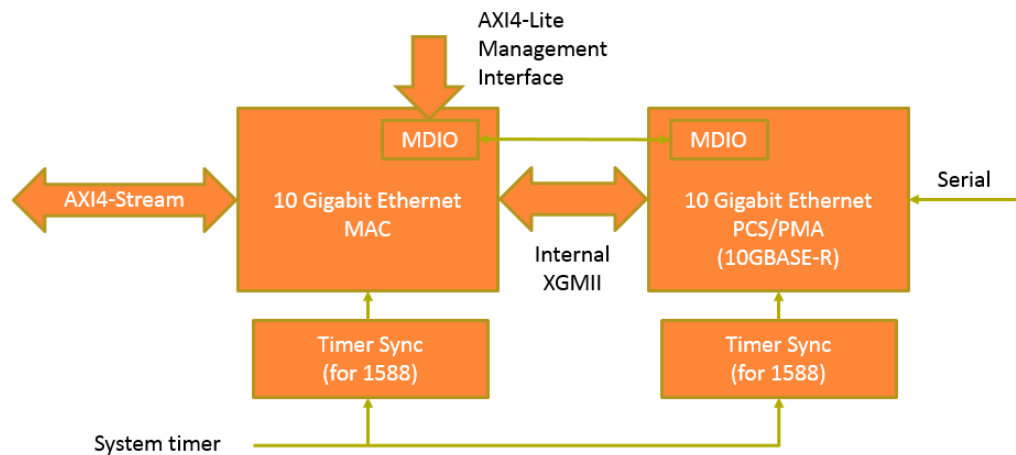

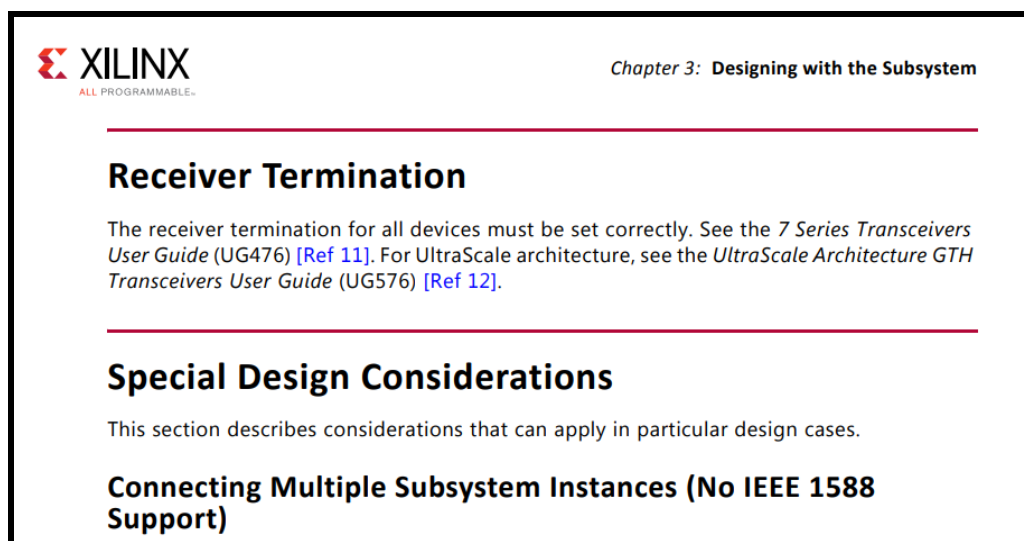**Figure 3-2: 10 Gb Ethernet High-Level Block Diagram.**

Figure 3-3: Xilinx Subsystem document screenshot [10].

To resolve this problem and the Xilinx IP core limitation, a new subsystem, called HPN subsystem, has been developed to support multiple IEEE-1588-v2 enabled subsystem. As it was mentioned before, the Xilinx approach uses time stamper unit for the transmit-side and the receiver-side inside the MAC and the PCS/PMA sub IP cores, respectively. Unlike the Xilinx approach, the developed HPN Subsystem uses a separate developed time stamper. Figure 3-4 shows the HPN Subsystem architecture. The HPN time stamper follows the same features as the Xilinx Subsystem. The time stamper unit is located between the MAC and PCS/PMA IP cores, uses the Timer Sync clock and follows the IEEE 1588 protocol. In addition, the time stamper considers the physical layer delay for stamping. Figure 3-5 shows the captured waveform of both transmit and the receiver sides after time stamping for loop-back case. In this scenario, the ingress and egress time stamps are both the same as the ones we used in the loop-back approach and therefore the residence time is zero.
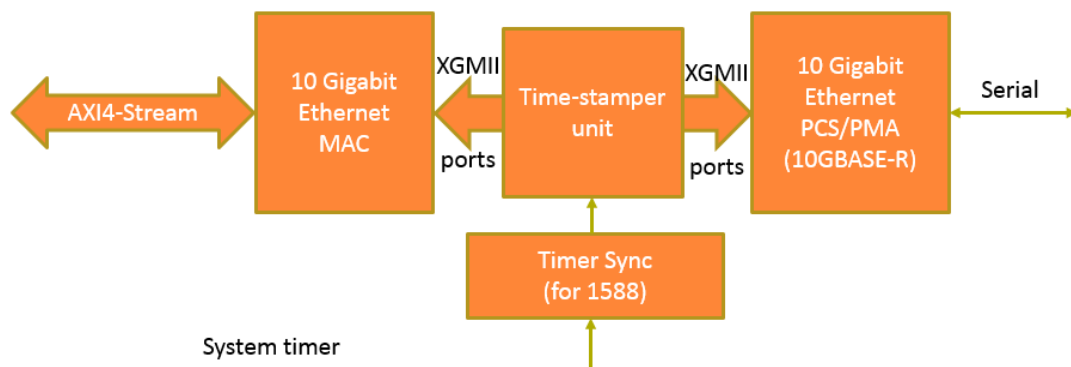

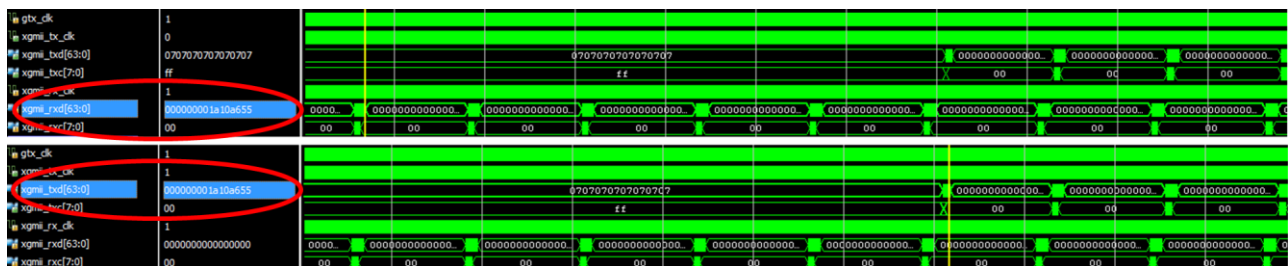**Figure 3-4: HPN Subsystem for synchronisation.**

Figure 3-5: Time stamp with HPN Subsystem for ingress and egress source node for loop-back scenario.

4 Backhaul Services over TSON – Supporting Ethernet

Extension of the TSON clients are only limited to the number of available transceivers on FPGA boards. We have extended the TSON Ethernet client ports to two for the 5G-XHaul solution, to support BH services based on the demonstration architecture defined in WP5.

Figure 4-1 shows the extended TSON solution to support BH service requirements in 5G. The multi-line client TSON follows the one client TSON legacy when the clients are using a different wavelength (i.e. λ). In addition, the Ethernet clients can use a common wavelength if the total bandwidth of the clients is less than 10 Gb/s. In this scenario, the packets are delivered to the related Ethernet clients at the egress nodes based on their header information (VLAN tag for 5G-XHaul [5]). This scenario fits well in the concept of the 5G-XHaul solution as the mmWave evaluation section [11] (deliverable D5.2, section 4.1.1) shows that the maximum achieved throughput for Typhoon module is 3.07 Gb/s.

Figure 4-2 shows the test scenario to validate and measure the latency of the extended TSON. As it can be seen in this figure, we have considered two scenarios: Loopback directly and using Bristol is Open (BIO) dark fibre. In both tests, each channel of the analyser sends 4.9 Gb/s Ethernet traffic with fixed frames of 1500B length to the TSON edge node. Then, from the other side, the traffic is aggregated to 9.8 Gb/s and is looped-back directly or via dark fibre available through the BIO test-bed. At the egress line, 9.8 Gb/s Ethernet traffic is segregated into two lines based on the VLAN tag and is transferred back to the analyser. Through these configurations error free performance was achieved. Figure 4-3 illustrates the measured latency based on the test scenarios. This table shows that the latency of TSON ingress and egress pipelines are less than 1μs in each direction.
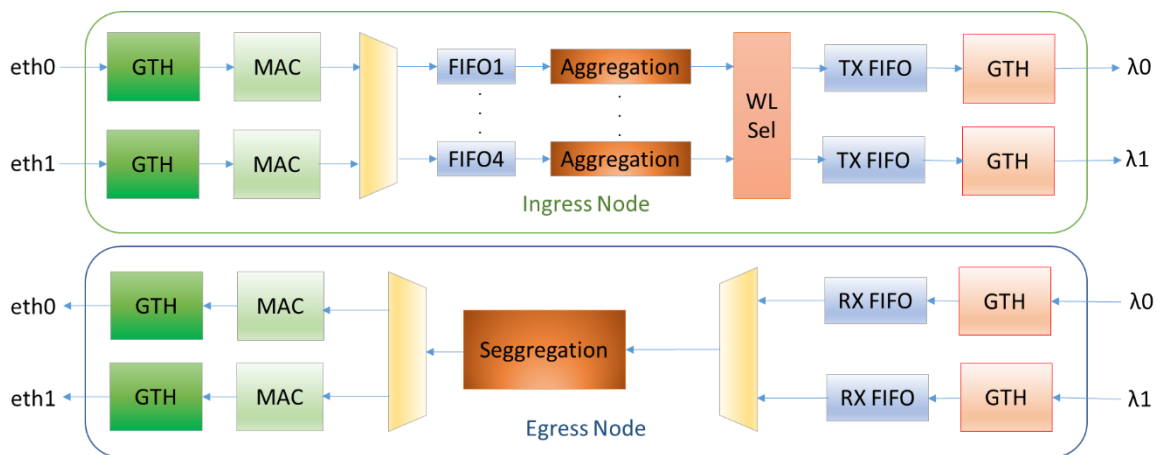

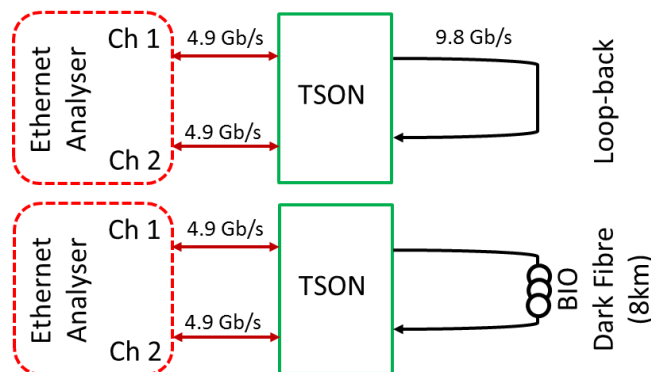**Figure 4-1: TSON extension for BH services with multi Ethernet clients.**

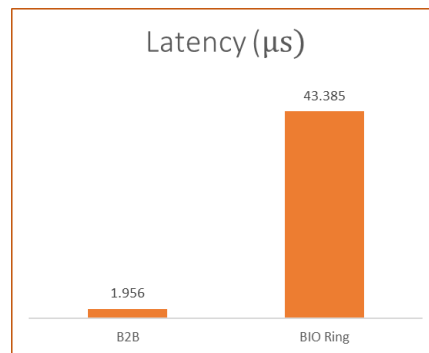**Figure 4-2: Extended TSON for BH test scenarios.**

Figure 4-3: Extended TSON for BH latency results.

5 Fronthaul Services over TSON – CPRI extension

Figure 5-1 shows the CPRI frame structure that sends sampled In-phase Quadrature (IQ) data in a frame format. The CPRI radio frame is 10 ms. CPRI line rate information is sent in Z.Y.W.X format between the Radio Unit (RU) and the Baseband Unit (BBU), where Z is the hyper frame number, Y is the basic frame within a hyper frame, W is the word number within a basic frame, and X is the byte number within a word. A single basic frame duration is 260 ns (1/3.84 MHz) which is compatible to a Universal Mobile Telecommunications System (UMTS) chip length. Each basic frame consists of 16 words, and the word length depends on the CPRI line rate: 256 basic frames make a hyper frame, and 150 hyper frames make a radio frame. CPRI supports topologies such as tree, ring, and chain, each link between RU and BBU is a fixed-bandwidth time-division-multiplexed (TDM) connection.

TSON's extension to enable native CPRI can support up to line rate option 5 with the current implementation as in 5G-XHaul the BBU and the Remote Radio Head (RRH) are using this option. The higher line rate option could use the same methodology for the TSON-CPRI integration. TSON can support varying service related requirements as its operational characteristics can be dynamically modified. Figure 5-2 illustrates how a heavy CPRI flows can be embedded into the TSON framing structure.

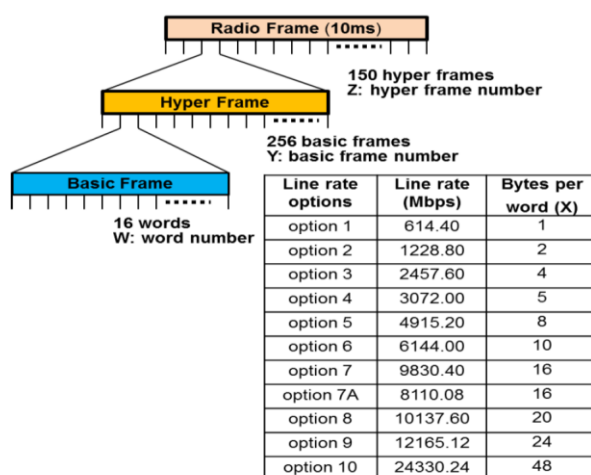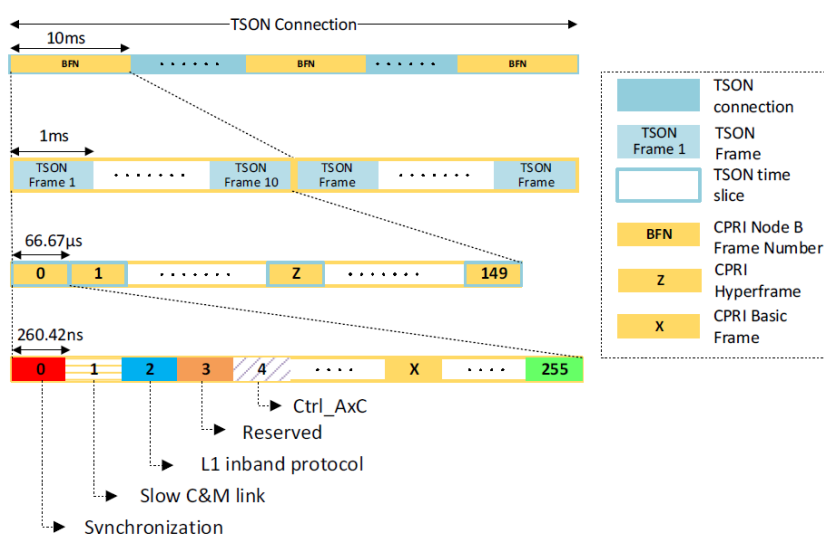| Line rate options	Line rate (Mbps)	Bytes per word (X)
option 1	614.40	1
option 2	1228.80	2
option 3	2457.60	4
option 4	3072.00	5
option 5	4915.20	8
option 6	6144.00	10
option 7	9830.40	16
option 7A	8110.08	16
option 8	10137.60	20
option 9	12165.12	24
option 10	24330.24	48

Figure 5-1: CPRI Frame Structure.

Figure 5-2: CPRI frame structure over TSON.

We have configured the Xilinx GTH Transceiver IP core for the CPRI protocol option 5. The reference clock frequency and data width for this IP core is 122.88 MHz and 32-bit respectively. The IP configuration uses 8B/10B encoding/decoding. Therefore, 4-bit control signals are available to indicate if data are special characters (comma symbols) or regular data for both the receiving and transmitting side. Comma symbols are used for synchronisation. The term of synchronisation here refers to finding the alignment of the 8b/10b codes within a bit-stream. Figure 5-3 shows the TSON edge node and CPRI integration high level architecture. In this architecture, the CPRI transceiver receives the CPRI frames and passes them to the *CPRI_TSON* interface unit in the ingress side. The *CPRI_TSON* interface is responsible for the Clock Domain Crossing (CDC) from 122.88 MHz to 156.25 MHz, which involves design the clock, and mapping the 32-bit data and 4-bit control to 64-bit corresponding to the TSON data width. Once the CPRI frames reach the aggregation block then according to the LUT information of the Time-slice Allocation, the aggregation block calculates the frames needed to construct the burst, aggregates the frames, waits for the valid Time-slice, and finally sends the burst into a different wavelength FIFO. The egress side has the reverse functionality.

As shown in Figure 5-4, the Anritsu traffic analyser (MT1100A) is used as the CPRI traffic generator and monitor to test the implemented design in an end-to-end mode using two TSON edge nodes.
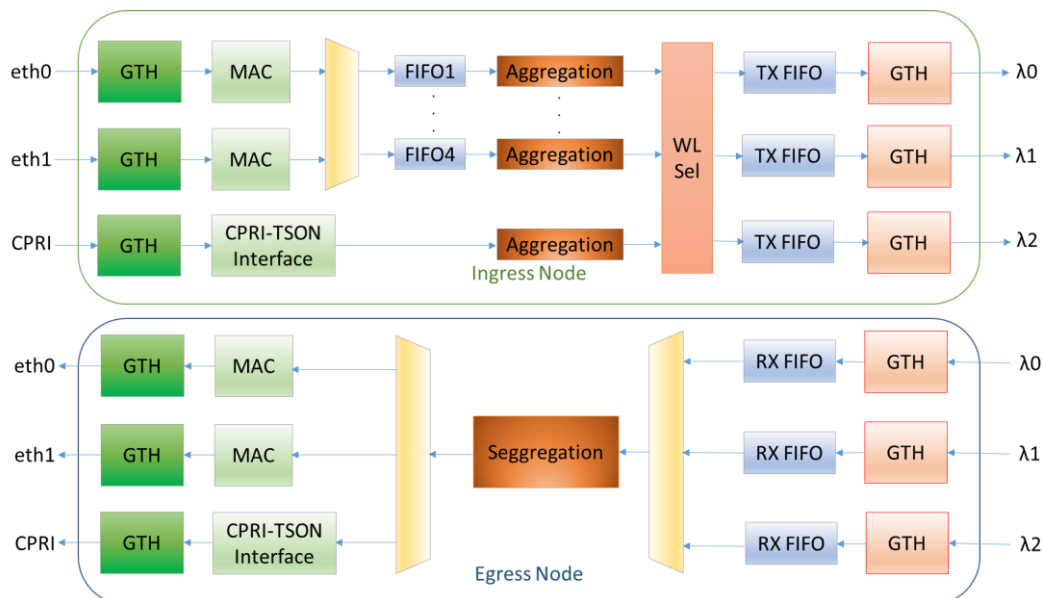

Figure 5-3: TSON edge node and CPRI integration high level architecture

Figure 5-4: CPRI end-to-end test using two TSON edge nodes.

6 TSON demonstration configuration

Figure 6-1 shows the TSON architecture for the 5G-XHaul final demonstration. As it can be seen in this figure, the configuration contains two TSON edge nodes. TSON edge node 1 is connected to three clients which are two Ethernet and one CPRI ports. TSON edge 2 is connected to two clients, a single Ethernet and one CPRI port.
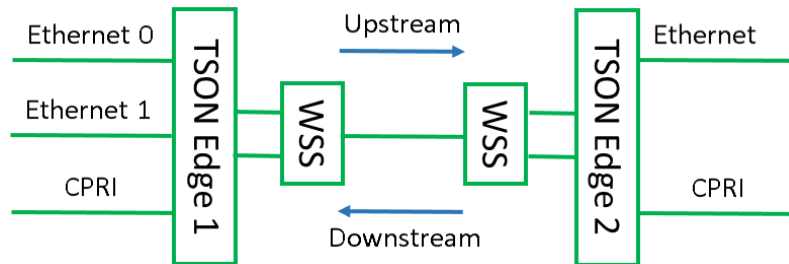

Figure 6-1: TSON architecture for 5G-XHaul final demonstration.

In the upstream scenario, the two Ethernet are aggregated into one flow and then are multiplexed together with the CPRI flow assigning to each a different wavelength. These two wavelengths are then fed into a Wavelength Selective Switch 1 (WSS 1). Then WSS 1 multiplexes the Ethernet and CPRI packets over a single fibre and send them to WSS 2. The WSS 2 receives the upstream and demultiplexes them into Ethernet and CPRI packet flows based on their wavelength. The TSON Edge 2 node receives the packets from the Ethernet and CPRI ports and passes them individually to their clients.

In the downstream scenario, the TSON Edge node 2 passes the Ethernet and CPRI packets each having a different wavelength to the WSS 2. The WSS 2 multiplexes the packets and pass them to WSS 1. Then, WSS1 demultiplexes the Ethernet and CPRI packets and passes them to the TSON Edge node 1. Finally, the CPRI traffic maps the CPRI client and the Ethernet traffic segregated to two Ethernet ports based on VLAN on the TSON Edge node 1. This architecture will be tested and evaluated by integrating TSON with ADVA's WDM-PON solution, and the Airrays' RRHs and TUD's BBU emulator before the final demonstration.

7   Resolving the technical Challenges

The NetFPGA SUME was chosen to implement the TSON based system at the beginning of this project. As it can be seen in Figure 7-1, this board has Four SFP+ interfaces. These interfaces are sufficient for one TSON client as the other three interfaces are connected to SDN, and two wavelengths can be used for internal TSON use. To integrate the Ethernet and CPRI clients, an external FPGA Mezzanine Card (FMC) module is required as the FMC connector on this board is directly connected to 10 GTH transceivers. The HiTechGlobal 10G/40G Ethernet FMC Module with customised oscillator to support CPRI IP core reference clock was purchased for this integration.
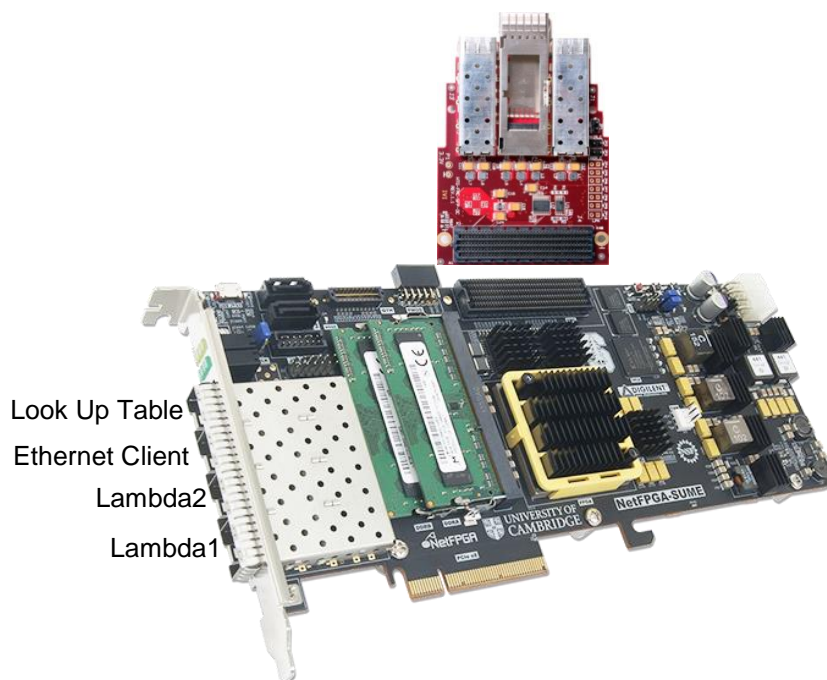

Figure 7-1: NetFPGA SUME FPGA board and HiTechGlobal 10G/40G Ethernet FMC module.

We had three major technical issues for this integration:

- The customised FMC card had an issue to produce the required clock for CPRI core. We have found this issue after several implementations and investigations. We returned the card and purchased a new FMC card from Faster Technology (Figure 7-2). This module has two quad-SFP cages and supports eight SFP/SFP+ transceiver modules that provides us sufficient I/O. Furthermore, after several investigations, we reached to realisation that the FMC card's clock is not sufficiently accurate for CPRI IP core due to its jitter performance. Then, we changed the design strategy to use on boards SFP+ s for CPRI and FMC cards for the Ethernet clients.

Figure 7-2: Faster Technology FMC Module.

- Although NetFPGA Sume is widely sold all around the world, its FMC hasn't been tested by an actual off the shelf FMC card module and the vendor claimed they have done only loopback tests based on their customised loopback board. We have debugged the NetFPGA Sume and we reached to the conclusion that there is an issue with the electrical connection inside this board as it successfully receives the packet but doesn't send them out. We asked for Digilent technical support via their forum about this issue. Unfortunately, they could not help us as it can be seen in Figure 7-3. To solve this issue, we have switched the TSON design to Xilinx vc709 evaluation board which is shown in Figure 7-4. The integration of the FMC module and vc709 evaluation board is working perfectly.

sbobrowicz ⊕ 68
Replied: December 11, 2017   Report reply
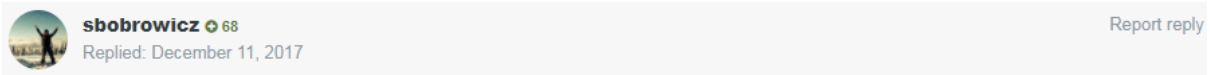
Our general policy is that we cannot purchase unsupported third party hardware in order to replicate customer issues in a support case. Doing so would be unsustainable in many situations. I've put a request into our demo content team for a demo that uses an SFP+ FMC Mezzanine card, but their is no guarantee that it will be prioritized to be completed any time soon.

sbobrowicz ⊕ 68
Replied: December 12, 2017   Report reply
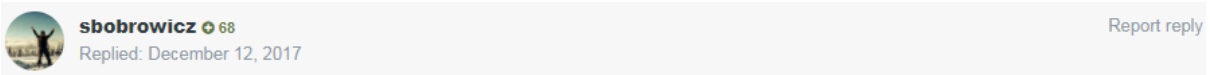
We make no guarantee that any third-party FMC mezzanine card will work with the SUME. It is up to you to integrate the card and get it working with the SUME. It may even be necessary for you to design your own FMC mezzanine card. We are available to assist you, but it is not our duty to do this job for you.

Figure 7-3: Digilent response to NetFPGA SUME issue.

Figure 7-4: Xilinx VC709 board.
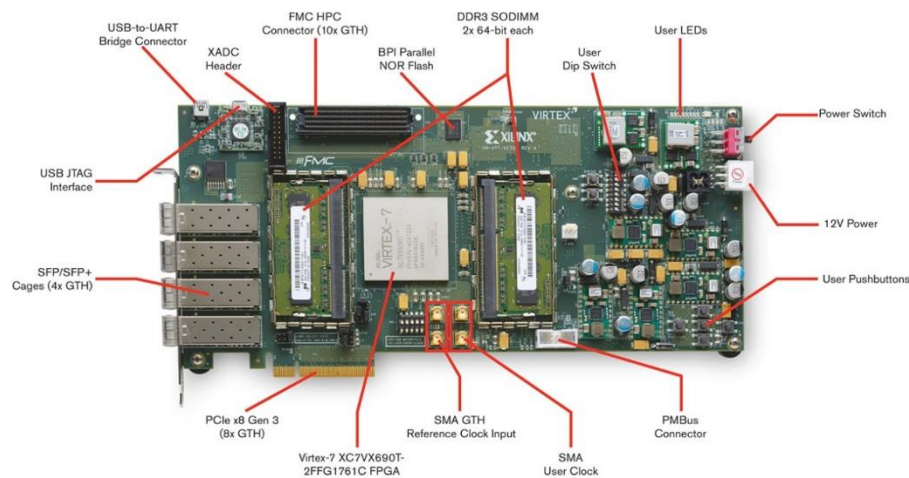
- The Xilinx GTH Transceiver needs a suitable jitter-attenuated recovered clock to drive the reference clock input of a GTH when the GTH is configured for CPRI. Traditionally an external clock with a specific recovery system is used to clock the CPRI core. We have managed to use on-board Silicon lab crystal for jitter-attenuation and clock recovery to avoid using external clock.

8 Summary and Conclusions

We have proposed TSON technology for the 5G-XHaul dynamic optical transport solution. In this document, we have discussed in detail TSON's architecture and functionality. In addition, we presented the TSON technology evaluation results. To become suitable to support FH and BH services in 5G-XHaul TSON needed several extensions such as synchronisation, supporting multi Ethernet clients for BH, and CPRI integration for FH services. We have developed the HPN synchronisation system to calculate the TSON network residence time based on the IEEE-1588 v2 standard and revealed the accuracy of the system through a loopback test scenario. We have extended the TSON for 5G-XHaul BH services by adding more Ethernet client ports able to be multiplexed and demultiplexed at the TSON edge nodes. This extension maintained all previous features of TSON and added increased functionality and flexibility to it by multiplexing two or more clients to one wavelength. This is the case when low bandwidth Ethernet clients are supported. We have tested and evaluated the new feature by loopback and the BIO dark fibre. TSON was also appropriately extended to support FH services. This feature was successfully implemented and tested using a traffic analyser and the TSON final demonstration configuration is presented based on the configuration provided by WP5 the demonstration related WP. We faced several technical challenges during the course of this work package which needed to be solved but have been able to address these issues successfully. It can be concluded that the extended TSON for 5G-XHaul solution is an enabling technology that can support converged FH and BH in 5G environments.

9 References

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10 Acronyms

Acronym	Description
BH	Backhaul
BBU	Baseband Unit
BIO	Bristol Is Open
CDC	Clock Domain Crossing
CPRI	Common Public Radio Interface
C-RAN	Centralised Radio Access Network
DC	Data Centre
EDFAs	Erbium Doped Fibre Amplifiers
FIFO	First In, First Out
FCS	Frame Check Sequence
FH	Fronthaul
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Arrays
IQ	In-phase Quadrature
LUT	Lookup Table
MAC	Medium Access Control
NIC	Network Interface Card
OBSAI	Open Base Station Architecture Initiative
PON	Passive Optical Network
QoS	Quality of Service
QoT	Quality of transmission
RAN	Radio Access Network
RRH	Remote Radio Head
RU	Radio Unit
TC	Transparent Clock
TDM	Time-Division-Multiplexed
ToD	Time-of-Day
TSN	Time Sensitive Networking
TSON	Time Shared Optical Network
UMTS	Universal Mobile Telecommunications System
VLAN	Virtual LAN
WSS	Wavelength Selective Switch